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SUBJECT Appeal Brief (10/076,357)

Number of Pages 18

Date 5/8/2006

MESSAGE

This fax transmission contains:

1. one copy of a Fax Transmittal Form;
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/076,357
Filing Date	02/14/2002
First Named Inventor	Dwip N Banerjee
Art Unit	2131
Examiner Name	Van Kim T. Nguyen
Attorney Docket Number	AUS920010893US1

Total Number of Pages in This Submission

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

Appeal Brief.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Volel Emile
Signature	
Date	05/08/2006

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Appl. No. 10/076,357
Fee Transmittal for Appeal Brief dated 05/08/2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of: Dwip N. Banerjee	
	Before the Examiner:
Serial No: 10/076,357	Van Kim T. Nguyen
Filed: 02/14/2002	Group Art Unit: 2151
Title: APPARATUS AND METHOD OF IMPROVING NETWORK PERFORMANCE USING VIRTUAL INTERFACES	Confirmation No.: 1515

TRANSMITTAL OF APPELLANTS' BRIEF UNDER 37 C.F.R. 1.192(a)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attached is Appellant's Brief from a decision of the Examiner dated **01/03/2006**, finally rejecting Claims 1 - 20.

The item(s) marked below are appropriate:

1. _____ A petition and fee for extension of term for reply to the final rejection is attached.
2. __X__ Appeal fee
   __X__ other than a small entity. Fee: $500.00
3. __X__ Payment
   __X__ Please charge Deposit Account **09-0447** the sum of $500.00. A duplicate of this notice is attached.

05/09/2006 HGUTEMA1 00000012 090447 10076357
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AUS920010893US1

Appl. No. 10/076,357
Fee Transmittal for Appeal Brief dated 05/08/2006

The Commissioner is hereby authorized to charge any additional fee, which may be required or credit any overpayment to Deposit Account No. **09-0447**.

Respectfully Submitted

By: _____
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Appl. No. 10/076,357
Appeal Brief dated 05/08/2006
Reply to Office Action of 01/03/2006

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Application of: Dwip N. Banerjee	
	Before the Examiner:
Serial No: 10/076,357	Van Kim T. Nguyen
Filed: 02/14/2002	Group Art Unit: 2151
Title: APPARATUS AND METHOD OF IMPROVING NETWORK PERFORMANCE USING VIRTUAL INTERFACES	Confirmation No.: 1515

APPELLANTS' BRIEF UNDER 37 C.F.R. 1.192

Assistant Commissioner of Patents
Washington, D. C. 20231

Sir:

This is an appeal to a final rejection dated January 03, 2006 of claims 1 - 20 of Application Serial Number 10/076,357 filed on February 14, 2002. This brief is submitted pursuant to a Notice of Appeal filed on March 08, 2006 in accordance with 37 C.F.R. 1.192.

BRIEF FOR APPLICANTS – APPELLANTS

(I)

Real Party in Interest

The real party in interest is International Business Machines Corporation (IBM), the assignee.

(II)

Related Appeals and Interferences

There are no other appeals or interferences known to appellants, appellants' representative or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(III)

Status of Claims

All claims in the Application (i.e., Claims 1 – 20) have been finally rejected.

(IV)

Status of Amendment

An amendment was filed subsequent to the Final Rejection. The amendment was directed toward the objection to the Drawings. By that amendment, Applicants have put the Application in condition for appeal.

(V)

Summary of Claimed Subject Matter

The present invention provides a method of improving performance in a multiprocessor system that uses a limited number of physical interfaces to transact network data. According to the teachings of the invention, when a multiprocessor system that uses a limited number of physical interfaces is to transact data, a determination is made as to whether the data is network data. If

the data is network data, the data is transmitted using a virtual Internet protocol (IP) address. The virtual IP address is the IP address of a data holding device rather than the address of a receiving computer (see page 14, line 18 to page 15, line 7 as well as Figs. 8 and 9).

(VI)

Grounds of Rejection to be Reviewed on Appeal

Whether the claims were properly rejected under 35 USC 102(e) as being anticipated by Potter.

(VII)

Arguments

In considering a Section 102 rejection, all the elements of the claimed invention must be disclosed in a single item of prior art in the form literally defined in the claim. *Jamesbury Corp. v. Litton Indus. Products*, 756 F.2d 1556, 225 USPQ 253 (Fed. Cir. 1985); *Atlas Powder Co. v. Dupont*, 750 F.2d 1569, 224 USPQ 409 (Fed. Cir. 1984); *American Hospital Supply v. Travenol Labs.*, 745 F.2d 1, 223 USPQ 577 (Fed. Cir. 1984).

Porter purports to teach a dynamic addressing mapping to eliminate memory resource contention in a symmetric multiprocessor system. According to Potter, the granularity of a dynamic random access memory (SDRAM) contention is typically one bank. A typical SDRAM module has four (4) banks, each containing a fixed one-quarter of the total memory. When a bank is accessed, it cannot be accessed again for a certain period of time (e.g., 7 cycles at 100 MHz). An SDRAM can support overlapping accesses to each of its banks, where new accesses can be issued every 2 cycles, but only one access at a time per bank is possible. To access relatively long table entries (e.g., entries containing words), the time that a bank is tied up increases, thereby directly

increasing access contentions. This can slow down a symmetric multiprocessor system that is configured as a multidimensional systolic array.

A systolic array is an array of processors which are connected to a small number of nearest neighbors in a mesh-like topology. For example, a one-dimensional systolic array may be regarded as a pipeline.

In a multidimensional systolic array, processors in the same position ("column") of each pipeline execute the same instructions on their input data. For a large class of applications including data networking, the processors in the same column access the same data structures. For example, a common table indicating a data communication queue must be accessible by all processors in the same column since it is not possible to know in advance which pipeline has the correct table for this input data. Therefore, access to a common memory is required among the processors of the same column.

To avoid contention and thus stalling by the processors, accesses to the common memory are scheduled. Since each processor of a column executes the same instruction code and therefore accesses the same tables in memory, the pipelines of the array are staggered (i.e., the array is configured such that a first processor of a first pipeline finishes accessing a particular memory just as a second processor of a second pipeline starts to access the same memory).

Since, however, only one access at a time per bank of an SDRAM is possible and since accesses to relatively long table entries may take up more than seven (7) cycles at 100 MHz, there will be access contentions. Potter devises a dynamic address mapping technique that eliminates contention to an SDRAM used by a symmetric multiprocessor system arranged as a multi-dimensional systolic array.

According to the teachings of Potter, the technique defines two logical-to-physical address mapping modes that may be simultaneously provided to the processors to thereby present a single contiguous address space for accessing individual memory locations: a bank select mode and a stream mode.

The bank select mode uses high-order address bits to select a bank of a memory resource for access. A data structure, such as a table having relatively short entries, is placed within a single bank of memory and addressed using the bank select mode. Assume that the bank is "tied up" for 7 cycles during an access to a single location in the table memory. A first processor in a first pipeline of the arrayed processing engine can access a random location within this table at absolute time N. As long as the skew between pipelines is as large as the time that the bank is tied up for a single access (i.e., 7 cycles), a second processor in the same column of a second pipeline can execute the same instructions (skewed by the 7 cycles). In this case, the second processor may access the same or a different location within the table (and bank) at time N+7 without contending with the first processor.

The stream mode uses low-order address bits to select a bank within a memory resource. Here, the data structure is preferably a table having relatively long entries, each containing words that are accessed over a plurality of cycles. According to this aspect, the long entries are spread across successive banks and stream mode addressing functions to map each successive word to a different bank. By defining the table entry width as a multiple of the access width times the number of banks, contentions can be eliminated.

For example, a processor of a first pipeline can access a first word of a random entry from a table resident in Bank 0 at absolute time N; that processor may then access a second word of the same entry from Bank 1 at time N+7. This process may continue with the processor "seeing" the entire entry as a contiguous address space. A corresponding processor of a next pipeline is skewed by 7 cycles and can execute the same instructions for accessing the same or different entry from the same table. Here, a first word is accessed from Bank 0 at time N+7, a second word is accessed from Bank 1 at time N+14, etc., without contention.

However, Potter does not teach, show or so much as suggest the steps of *determining whether data being processed is network data;* and *of transacting, if*

the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address of a data holding device as claimed.

Therefore, Applicants submit that the claims are allowable. Hence, reconsideration, allowance and passage to issue of the claims are respectfully requested.

Respectfully Submitted

By:

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(VIII)

Claims Appendix

1. (Previously amended) A method of improving performance in a multiprocessor system that uses a limited number of physical interfaces to transact network data comprising the steps of:

determining whether data being processed is network data; and

transacting, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system.

2. (Previously amended) The method of Claim 1 wherein the data holding device is a buffer.

3. (Original) The method of Claim 2 wherein the buffer is implemented using memory allocation.

4. (Original) The method of Claim 3 wherein the buffer contends for access to one of the limited physical interfaces.

5. (Original) The method of Claim 4 wherein before transmitting the data to the physical interface, the virtual IP address is replaced by a destination IP address.

6. (Previously amended) A computer program product on a computer readable medium for improving performance of a multiprocessor system that uses a limited number of physical interfaces to transact network data comprising:

code means for determining whether data being processed is network data; and

code means for transacting, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system.

7. (Previously amended) The computer program product of Claim 6 wherein the data holding device is a buffer.

8. (Original) The computer program product of Claim 7 wherein the buffer is implemented using memory allocation.

9. (Original) The computer program product of Claim 8 wherein the buffer contends for access to one of the limited physical interfaces.

10. (Original) The computer program product of Claim 9 wherein before transmitting the data to the physical interface, the virtual IP address is replaced by a destination IP address.

11. (Previously amended) An apparatus for improving performance of a multiprocessor system that uses a limited number of physical interfaces to transact network data comprising:

means for determining whether data being processed is network data; and

means for transacting, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system.

12. (Previously amended) The apparatus of Claim 11 wherein the data holding device is a buffer.

13. (Original) The apparatus of Claim 12 wherein the buffer is implemented using memory allocation.

14. (Original) The apparatus of Claim 13 wherein the buffer contends for access to one of the limited physical interfaces.

15. (Original) The apparatus of Claim 14 wherein before transmitting the data to the physical interface, the virtual IP address is replaced by a destination IP address.

16. (Previously amended) A multiprocessor system having means for improving performance comprising:

at least one memory device to store code data; and

using one of the processors processor for processing the code data to determine whether data being processed is network data and to transact, if the data is network data, the data using a virtual Internet protocol (IP) address, the virtual IP address being an IP address given to a data holding device in the multiprocessor system.

17. (Previously amended) The multiprocessor system of Claim 16 wherein the data holding device is a buffer.

18. (Original) The multiprocessor system of Claim 17 wherein the buffer is implemented using memory allocation.

19. (Original) The multiprocessor system of Claim 18 wherein the buffer contends for access to one of the limited physical interfaces.

20. (Original) The multiprocessor system of Claim 19 wherein before transmitting the data to the physical interface, the virtual IP address is replaced by a destination IP address.

(IX)

Evidence Appendix

No evidence was submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 and 1.132 nor was there any evidence entered by the Examiner relied upon by Appellants in this appeal.

(X)

Related Proceedings Appendix

There are no decisions rendered by a court or the Board that would have a bearing on the Board's decision in the pending appeal.